AMENDMENTS TO THE SPECIFICATION:

Due to the number of typographical errors in the originally filed specification, a substitute specification is being concurrently submitted in compliance with MPEP §608.01(q). The substitute specification does not include new matter. Applicant is providing the Examiner with a marked up version of the substitute specification showing all the changes to the specification of record. Applicant is also submitting a clean version of the specification without markings.

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SPECIFICATION

An optimum UMTS Modem for multimedia Data, Voice, VoIP

in wireless Internet applications.

Cross Reference to Related Applications

Referenced-applications

This application is related to co-pending U.S. patent

application number 09/681093, filed Jan. 2, 2001, and

entitled "Turbo Codes Decoder".

Background of Invention

Field of the Invention

[0001]   This invention relates to a Universal Mobile

Telecommunications System (UMTS) Modem for third

generation (3G) Wireless Mobile Communications; and

more particularly, to a very high speed UMTS Modem

using a Turbo Codes Encoder/Decoder and channel

hopping with an Orthogonal Frequency Division

Multiplexing method implemented by complex fast

Fourier transform (FFT)/inverse fast Fourier

transform (iFFT) processors for multimedia Data,

Voice, Voice over Internet Protocol (VoIP) in

wireless Internet applications.

Description of the Prior Art

[0002]   UMTS stands for a Universal Mobile

Telecommunications System.   UMTS is part of the IMT-

2000, a global family of 3G mobile communications

systems delivering high-value broadband information,

commerce and multimedia entertainment services to

mobile users via fixed, wireless and satellite

Internet Protocol (IP) networks.   Modem stands for

modulation and demodulation.   When a base station

sends digital information to the terminal handset,

the modem at the base station converts the digital

data into an analog signal and transmits the analog

signal over the air, and the terminal handset modem

receives the analog signal and converts the analog

signal back into digital data.   As shown in FIGURE

1, digital data from the Media Access Control (MAC)

layer 15 is shifted into the UMTS modem transmitter

where data is encoded for error-correction.   The

data is modulated and sent to the analog front-end

16 for transmission over the air.   Received signals

from the analog front-end 16 enter the UMTS modem

receiver 13 where they are demodulated by a baseband

processor, then shifted to the MAC layer 15.   The

Turbo Codes baseband processor is used to encode

data and to reconstruct the received data that is

2

corrupted and noisy and to improve bit-error-rate (BER) data throughput in a limited power and noisy environment. The Orthogonal Frequency Division Multiplexing is a technique used to divide the broadband channel into sub-channels where multiple adjacent channels transmit their carriers' frequency, which are orthogonal to each other. The sum of all carriers can be transmitted over the air to the receiver where each channel's carrier can be separated without loss of information due to interferences. FIGURE 2 shows an example of an 8-PSK constellations where each group of 3-bit data is mapped in to a point with in-phase (I) and quadrature-phase (Q) coordinates.

Summary of Invention

[0003]   The invention provides improved methods and architecture of an UMTS modem for delivering optimum high-speed broadband information, commerce and multimedia entertainment services to mobile users via fixed, wireless and satellite IP networks. The invention utilizes Turbo Codes baseband processors for optimum performance in decoding received data in limited power and noisy environments. The invention

presents a method to divide the UMTS broadband into multiple sub-channels and uses an Orthogonal Frequency Division Multiplexing method implemented by N-point complex FFT/iFFT processors to effectively divide the broadband high-speed channel into multiple slow-speed N sub-channels where multiple adjacent channels transmit their carriers' frequency which are orthogonal to each other. The high-speed bit-stream is also sub-divided into multiple slow-speed sub bit-streams. For example, if the total broadband channel capacity is R-Mbps, then the slower sub-channel capacity S-Mbps is equal to (R-Mbps)/N. The slower sub-channel capacity improves the Turbo Codes baseband processor since it performs much better at a slower bit rate with a greater number of iterations. The invention utilizes an M-bit serial-to-parallel (S/P) converter to sub-divide the input high-speed R-Mbps bit-stream into multiple M slow-speed S-Mbps bit-streams, where each bit-stream will be transmitted in the assigned channel. Each bit-stream is encoded one bit per cycle with the Turbo Codes encoder and then mapped into an 8-PSK constellation point where its I and Q components are mapped into the real and imaginary part of the complex iFFT point. Since M is

4

less than or equal to N, channel hopping can be accomplished by assigning a bit-stream to a new channel once its current channel becomes noisy. Accordingly, several objects and advantages of the invention are:

[0004]   To deliver high-quality, high-speed broadband information to the wireless IP network.

[0005]   To utilize the Turbo Codes baseband processor, rate 1/3, 8-state SISO Log-MAP, for optimum performance in decoding received data.

[0006]   To utilize an M-bit serial-to-parallel (S/P) converter to sub-divide the input high-speed bit-stream into multiple M slow-speed bit-streams.

[0007]   To utilize an Orthogonal Frequency Division Multiplexing method implemented by N-point complex FFT/iFFT processors to sub-divide the broadband high-speed channel into multiple slow-speed N sub-channels.

[0008]   To implement channel hopping to re-assign a new channel once the existing channel becomes noisy.

[0009]   To utilize a guard-interval (GI) addition to minimize intersymbol interference.

[0010]   Still further objectives and advantages will become apparent to one skill in the art from a consideration of the ensuing examples, descriptions

5

and accompanying drawings.

Brief Description of Drawings

[0011]   FIGURE 1 illustrates an UMTS Modem System Block

Diagram (Prior Art).

[0012]   FIGURE 2 illustrates an 8-PSK Constellations

(Prior Art).

[0013]   FIGURE 3 illustrates an UMTS Modem Transmitter

Functional Block Diagram.

[0014]   FIGURE 4 illustrates an UMTS Modem Receiver

Functional Block Diagram.

Detailed Description

[0015]   As shown in FIGURE 1, an UMTS modem 11 comprises

a modem transmitter 12 for modulating digital data and

sending the signal over the air, a modem receiver 13

for demodulating received signals and converting the

received signals into digital data, and an AFC Clock

Recovery circuit for recovering clock and

synchronization information.

UMTS Modem Transmitter

[0016]   As shown in FIGURE 3, an UMTS modem transmitter

12 comprises an M-bit serial-to-parallel (S/P)

converter 31 to convert an inputted bit-stream

into an M number of sub bit-streams, an M number

of Turbo Codes encoders 32 with coding rate 1/3
and constraint length K=4 corresponding to each
bit-stream, an M number of Mappers 33 for 8-PSK
modulation corresponding to each channel, a
Channel Selector for assigning each bit-stream to
a sub-channel, an N-point complex iFFT processor
34 for implementing multiple sub-channels with
Orthogonal Frequency Division Multiplexing
methods, a guard interval (GI) adder 35 for
adding guard interval, a Symbol Wave Shaper 36,
and an IQ Modulator 37 for modulating the
transmitted signal with a carrier, and a Carrier
generator 38 that produces a carrier frequency.

[0017]   As shown in FIGURE 3 and in FIGURE 1, the UMTS
modem transmitter 12 functions effectively as
follows:

[0018]   High-speed R-Mbps input serial data is shifted
into the M-bit serial-to-parallel (S/P) converter
31 to generate the slow-speed S-Mbps M parallel
sub bit-streams (labeled from 0 to M-1).

[0019]   Each sub bit-stream is shifted serially into
its own Turbo Codes encoder 32, with coding rate
1/3 and constraint length K=4, one bit per cycle
where it is converted into a 3-bit symbol output

7

(one data bit and two parity bits).

[0020]   The 3-bit symbol 22 is shifted into the 8-PSK
Mapper 33 where it is mapped into a constellation
point 21 as shown in FIGURE 2. The values of its
I and Q components are selected from the Table 1.
The output of the 8-PSK Mapper 33 is a set of
(I,Q) values that correspond to the Real and
Imaginary parts of a point in the complex iFFT
processor.

[0021]   The (I,Q) values are shifted into the Channel
Selector 39 where each set of (I,Q) is assigned
to a point in the N-point complex iFFT processor.
When channel hopping is required, the Channel
Selector 39 can re-assign a new point for the
requested set of (I,Q).

[0022]   The complex iFFT Processor 34 performs the
complex inverse fast Fourier transform (iFFT) to
produce N complex samples which are then
separated into an I sequence and a Q sequence of
N samples that correspond to the real and
imaginary parts.

[0023]   The I and Q sequences are shifted completely
through the GI Adder 35 where the guard interval
is added to each I and Q sequences.

8

[0024]   The I and Q sequences are then shifted
completely through the Symbol Wave Shaper 36
where the I and Q sequences are modified by a
symbol wave-shaper FIR filter.

[0025]   The I and Q sequences are then shifted
completely through the IQ Modulator 37 where the
I sequence is modulated with Sine carrier 38, and
the Q sequence is modulated with a Cosine carrier
38. The summation of the modulated I and Q
sequences produces the transmitted signal output.

UMTS Modem Receiver

[0026]   As shown in FIGURE 4, an UMTS modem receiver
13 comprises an IQ demodulator 41 for demodulating
the received signal with a carrier, a local carrier
generator 48 produces carrier frequency, an AFC
Clock circuit 47, a guard interval (GI) remover 42
for deleting guard interval, an N-point complex FFT
processor 43 for implementing multiple sub-channels
with a Orthogonal Frequency Division Multiplexing
method, an M number of de-Mappers 44 for 8-PSK
demodulation corresponding to each channel, an M
number of Turbo Codes Decoder baseband processors
45 with coding rate 1/3 and constraint length K=4
corresponding to each bit-stream, an M-bit

9

parallel-to-serial (P/S) converter 46 to convert the M input sub bit-streams into a final bit-streams output.

[0027]   As shown in FIGURE 4 and FIGURE 1, the UMTS modem receiver 13 functions effectively as follows:

[0028]   Received signals entering the IQ Demodulator 41 are demodulated with a local carrier 48 to produce the I and Q sequences of N samples.

[0029]   The I and Q sequences are shifted completely through the GI Remover 42 where the guard interval is remove from each I and Q sequence.

[0030]   The I and Q sequences are then shifted completely into the N-point complex FFT Processor 43. The FFT Processor 43 performs the complex Fast Fourier Transform (FFT) for the I and Q sequences of N samples to convert them into N complex points of data.

[0031]   The Channel De-selector 49 then selects each complex point of data for each set of (I,Q) values that correspond to each of the M bit-streams.

[0032]   Each set of (I,Q) is shifted into the 8-PSK De-Mapper 44 where it is converted into a soft-decision value output.

[0033]   The soft-decision value data is shifted into

the Turbo Codes Decoder baseband processor 45, where data is iteratively decoded until a final decision hard-decoded bit is produced for the output that correspond to each bit-stream.

[0034]   The hard-decoded output bit is latched into the M-bit parallel-to-serial (P/S) converter 46, where all the M-bit data is serially shifted to the output.

Claims

[c1] An optimum UMTS Modem for multimedia Data, Voice,

VoIP in wireless Internet applications comprising of:

an UMTS modem transmitter;

an UMTS modem receiver;

an N-point complex FFT processor and an N-point complex

iFFT processor for implementing the multiple sub-

channels with Orthogonal Frequency Division

Multiplexing method;

a Turbo Codes baseband processor for optimum

performance in decoding of noisy receive data, and

encoding transmit data;

an 8-PSK Mapper for mapping a 3-bit symbol into a point

on the 8-PSK constellations with the I and Q component

values;

an 8-PSK De-mapper for converting the received set

(I,Q) values from the complex FFT processor into soft-

decision values for the Turbo Code baseband processor;

an M-bit serial-to-parallel (S/P) converter for

segmenting the input bit-stream into an M number of sub

bit-streams;

an M-bit parallel-to-serial (P/S) converter for

shifting the decoded data to the output;

a Channel Selector and a Channel De-selector for

assigning bit-streams into sub-channels, and also

controlling the channel hopping function;

a GI adder and a GI remover for adding and removing

guard intervals from the I and Q sequences of samples;

a Symbol wave shaper;

an IQ Modulator for modulating the I and Q sequences of

samples and adding them into a transmit signal;

an IQ Demodulator for demodulating the receive signal

and producing the I and Q sequences of N samples; and

an AFC Clock Recovery circuitry for clock synchronization.

[c2] The UMTS modem system of claim c1, wherein the Turbo

Codes baseband processor uses SISO 8-state Log-MAP

decoder for high-speed and optimum decoding a

plurality of sequences of the receive samples.

[c3] The UMTS modem system of claim c1, wherein the 8-PSK

De-mapper produces soft-decision values output.

[c4] The UMTS modem system of claim c1, wherein the complex

FFT/iFFT processors sub-divide the UMTS broadband

channel into multiple sub-channels by using the

Orthogonal Frequency Division Multiplexing method.

[c5] The UMTS modem system of claim c1, wherein the M-bit

serial-to-parallel (S/P) converter sub-divides the

high-speed R-Mbps input to generate the multiple slow-

speed S-Mbps M sub bit-streams; where S-Mbps is equal

13

to R-Mbps divide by N.

[c6] The UMTS modem system of claim c1, further provides a
method to divide the UMTS broadband into multiple sub-
channels and the uses of an Orthogonal Frequency
Division Multiplexing method implemented by N-point
complex FFT/iFFT processors where multiple adjacent
channels transmit their carriers' frequency which are
orthogonal to each other.

[c7]   The
UMTS modem system of claim c1, further provides a
method to divide high-speed bit-stream into multiple
slow-speed sub bit-streams for transmitting over the
sub-channels.

[c8] The UMTS modem system of claim c1, further provides a
method to control channels hopping by re-assign
bitstream into another sub-channel.

[c9]   A method for UMTS modem transmitting a plurality
of high-speed digital information generated from a MAC
layer into wireless IP networks comprising the steps
of:

(1) sub-divide the high-speed R-Mbps input serial data by
shifting it into the M-bit serial-to-parallel (S/P)
converter to generate the multiple slow-speed S-Mbps M
sub bit-streams;

(2) encode each bit of each bit-streams independently with
    a Turbo Codes encoder, with coding rate 1/3 and
    constraint length K=4, to generate a 3-bit symbol (one
    data bit and two parity bits);

(3) map the 3-bit symbol into an 8-PSK constellations
    points to select the values of its I and Q components;

at this point, all the sub bit-streams are done the same as
    the above step (2), (3);

(4) select a point in the N-point complex iFFT and map the
    I component into its real part and the Q component
    into its imaginary par accordingly;

(5) perform the invert complex N-point Fast Fourier
    Transform to produces the two I and Q sequences of N
    samples corresponding to the real and imaginary of the
    complex iFFT products;

(6) add the guard interval to the I and Q sequences of N
    samples;

(7) modify the I and Q sequences of N samples with and FIR
    filter Symbol wave shaper;

(8) modulate the I sequence with a Sine carrier, and the Q
    sequence with a Cosine carrier;

(9) sum the two modulated I and Q with an adder to produce
    the transmit signal.

[c10]   A method for UMTS modem receiving a plurality of

15

high-speed digital information received from the
wireless IP networks comprising the steps of:

(1) demodulate the receive signal with a local carrier to
produce the I and Q sequences of N samples;

(2) remove the guard interval from the I and Q sequences of
N samples;

(3) perform the complex N-point Fast Fourier Transform on
the I and Q sequences of N samples to convert them
into N complex points data;

(4) de-selector each of N complex point data for each set
of (I,Q) values correspond to each of the M bit-
streams;

(5) de-map each of the M complex point (I,Q) based on an 8-
PSK constellations to produce soft-decision values;

(6) decode the soft-decision value with the Turbo Codes
Decoder baseband processor, where data is iteratively
decoded until a final decided hard-decoded bit is
produced for the output correspond to each bit-stream;
at this point, all bit-streams are done with steps (5) and
(6);

(7) latch all M decoded bits into the parallel-to-serial
converter and shift out to the output.

Abstract of Disclosure

The invention encompasses systems and methods associated with an UMTS modem for delivering optimum high-speed broadband information, commerce and multimedia entertainment services to mobile users via fixed, wireless and satellite IP networks. The invention utilizes a Turbo Codes baseband processor for optimum performance in decoding received data in limited power and noisy environments. The invention provides a method for dividing the high-speed bit-stream into multiple slow-speed sub bit-streams, and also dividing the UMTS broadband channel into multiple sub-channels for transmitting each sub bit-stream in the assigned adjacent sub-channels, and uses the Orthogonal Frequency Division Multiplexing method implemented by N-point complex FFT/iFFT processor to effectively divide the broadband high-speed channel into multiple slow-speed N sub-channels where multiple adjacent channels transmit their carriers' frequency which are orthogonal to each other. Also, when M is smaller than N, channel hopping can be done by re-assigning a bit-stream to another sub-channel slot.